

I²C Controlled 2.5A / 4.5A Single Cell USB/Adapter Charger With 5.1V at 1A / 5.1V at 2.1A Synchronous Boost Operation

Check for Samples: bq24195, bq24195L

FEATURES

- High Efficiency Switch Mode Charger
  - 2.5A(bq24195L) or 4.5A(bq24195) Fast Charging
  - 92% Charge Efficiency at 2A, 90% at 4A
- Synchronous Boost Converter in Battery Boost Mode
  - 5.1V at 1A (bq24195L) or 5.1V at 2.1A (bq24195)
  - 94% 5.1V Boost Efficiency at 1A, 91% at 2.1A
- Highest Battery Discharge Efficiency with 12mΩ Battery Discharge MOSFET up to 9A Discharge Current
- Single Input USB-compliant/Adapter Charger
  - USB Host or Charging Port D+/D- Detection Compatible to USB Battery Charger Spec 1.2
  - Input Voltage and Current Limit Supports USB2.0 and USB 3.0
  - Input Current Limit: 100mA, 150mA, 500mA, 900mA, 1.2A, 1.5A, 2A and 3A
- 3.9V–17V Input Operating Voltage Range
  - Support All Kinds of Adapter with Input Voltage DPM Regulation
- Narrow VDC (NVDC) Power Path Management
  - Instant-on Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- 1.5MHz Switching Frequency for Low Profile Inductor
- Autonomous Battery Charging with or without Host Management
  - Battery Charge Enable
  - Battery Charge Preconditioning
  - Charge Termination and Recharge
- High Accuracy (0°C to 125°C)
  - ±0.5% Charge Voltage Regulation
  - ±7% Charge Current Regulation
  - ±7.5% Input Current Regulation
  - ±2% Output Regulation in Boost Mode
- High Integration
  - Power Path Management
  - Synchronous Switching MOSFETs
  - Integrated Current Sensing
  - Bootstrap Diode
  - Internal Loop Compensation
- Safety
  - Battery Temperature Sensing and Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input System Over-Voltage Protection
  - MOSFET Over-Current Protection
- Charge Status Outputs for LED or Host Processor
- Low Battery Leakage Current and Support Shipping Mode
- 4mm x 4mm QFN-24 Package

APPLICATIONS

- Power Bank for Smartphone, Tablet
- Tablet PC
- Smart Phone
- Portable Audio Speaker
- Portable Media Players
- Internet Devices







These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The bq24195L, bq24195 are highly-integrated switch-mode battery charge management and system power path management devices for single cell Li-Ion and Li-polymer battery in a wide range of power bank, tablet and other portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port and high power DC adapter. To set the default input current limit, the bq24195L, bq24195 detects the input source following the USB battery charging spec 1.2. The bq24195/bq24195L are compliant with USB 2.0 and USB 3.0 power specifications with input current and voltage regulation. The bq24195L, bq24195 supports battery boost operation by supplying 5.1V on PMID pin with minimum current of 1.0A (bq24195L) or 2.1A (bq24195).

The power path management regulates the system slightly above battery voltage but does not drop below 3.5V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This supplement mode operation prevents overloading the input source.

The devices initiate and complete a charging cycle without software control. It automatically detects the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The devices provide various safety features for battery charging and system operation, including negative thermistor monitoring, charging safety timer and over-voltage/over-current protections. The thermal regulation reduces charge current when the junction temperature exceeds 120°C (programmable).

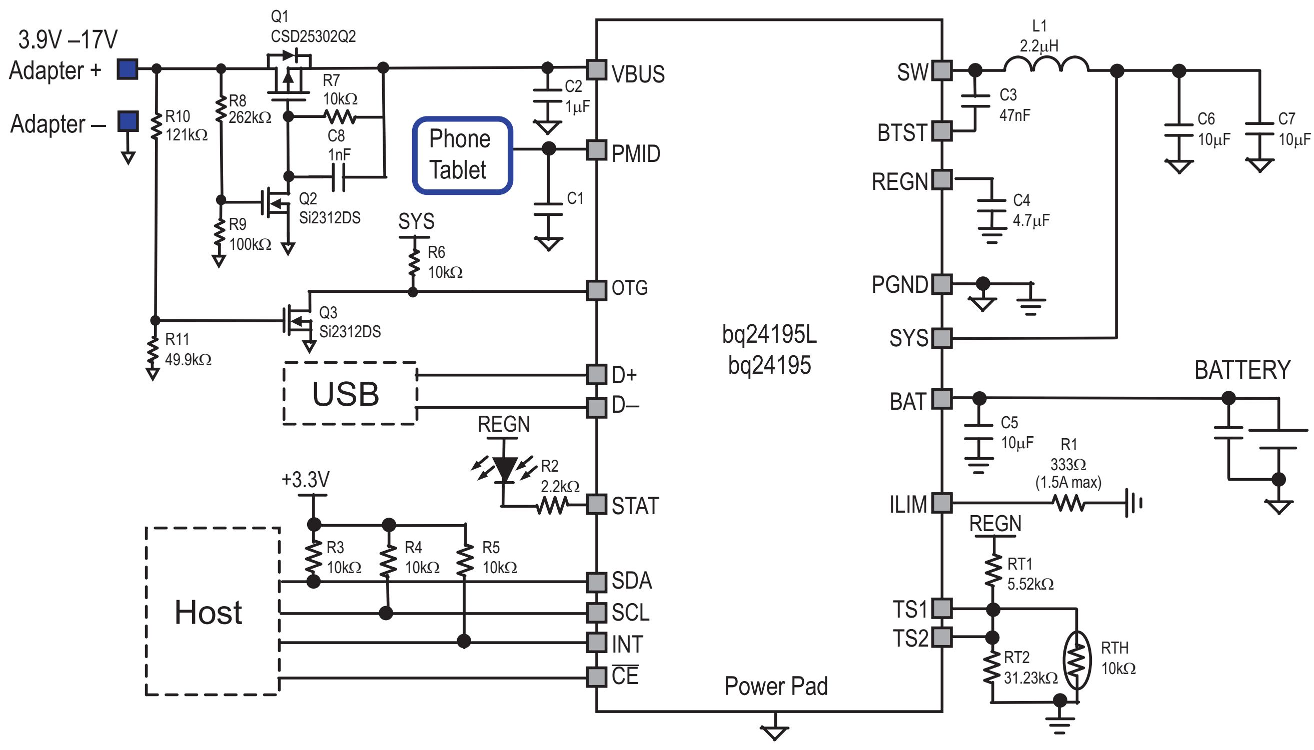
The STAT output reports the charging status and any fault conditions. The INT immediately notifies the host when a fault occurs.

The bq24195 and bq24195L are available in a 24-pin, 4x4 mm^2 thin QFN package.

ORDERING INFORMATION

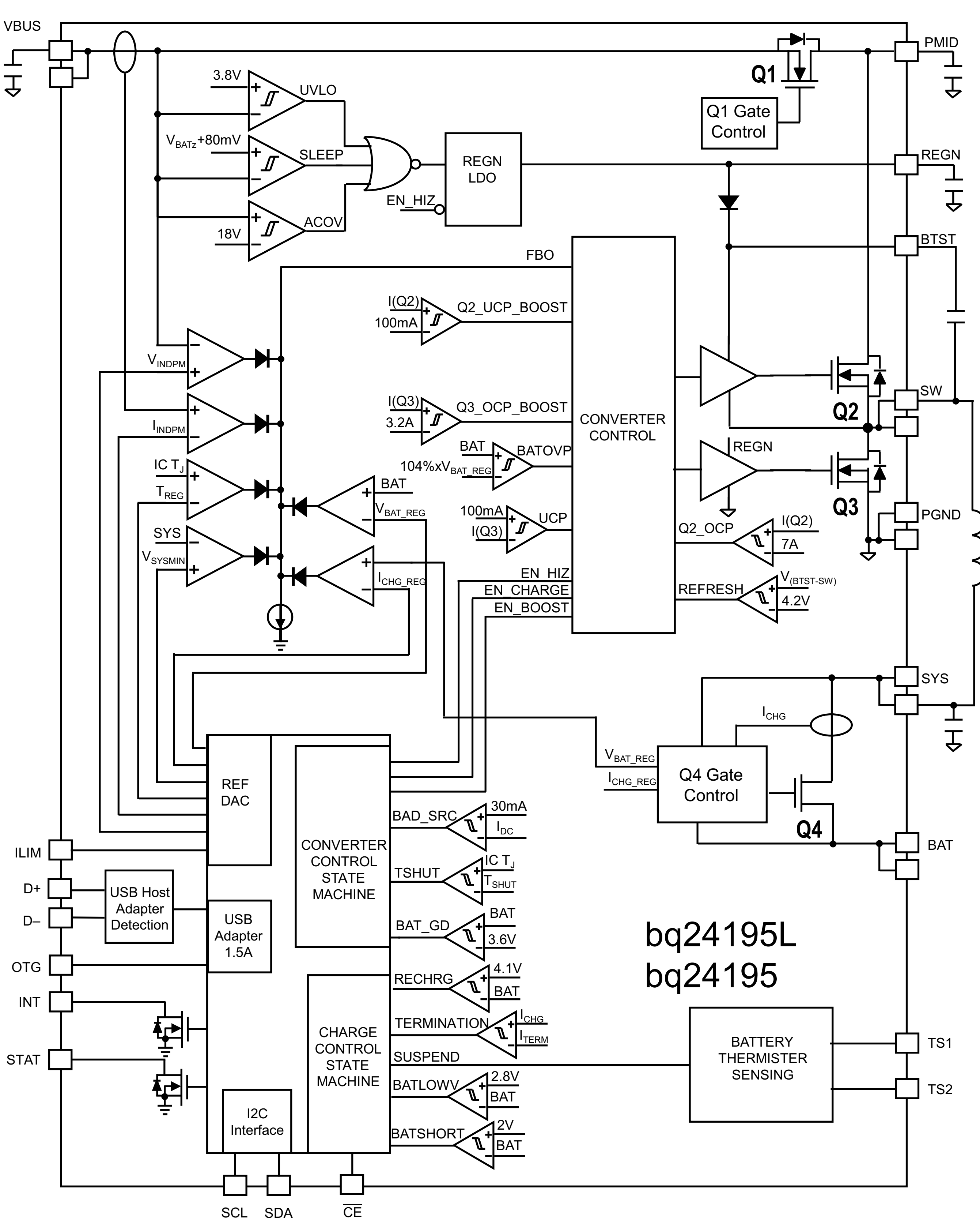
PART NUMBER	PART MARKING	PACKAGE	ORDERING NUMBER	QUANTITY
bq24195	bq24195	24-pin 4mmx4mm VQFN	bq24195RGER	3000
			bq24195RGET	250
bq24195L	bq24195L	24-pin 4mmx4mm VQFN	bq24195LRGER	3000
			bq24195LRGET	250

APPLICATION SCHEMATIC

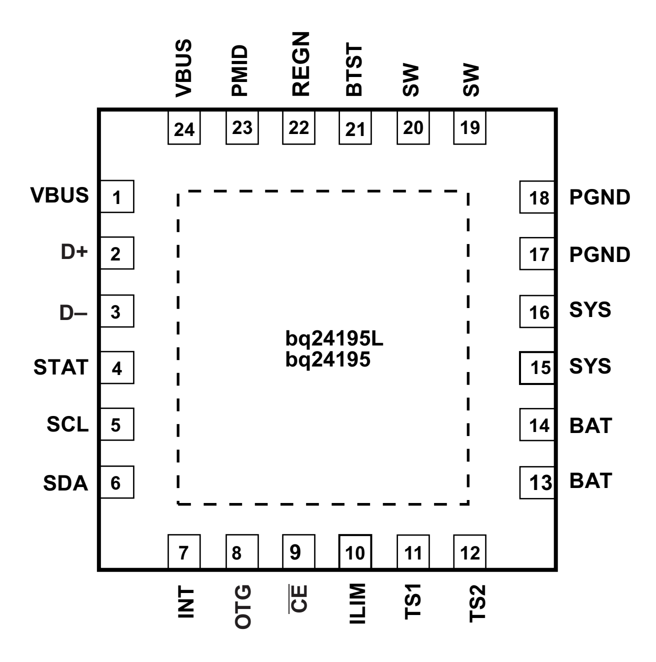


Recommended C1(min) = 20µF (bq24195L) or 60µF (bq24195)

FUNCTIONAL BLOCK DIAGRAM



PINOUTS



PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
VBUS	1,24	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. (Refer to Application Information Section for details)
D+	2	I Analog	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
D–	3	I Analog	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
STAT	4	O Digital	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kohm. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks at 1Hz.
SCL	5	I Digital	I^2C Interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	6	I/O Digital	I^2C Interface data. Connect SDA to the logic rail through a 10kΩ resistor.
INT	7	O Digital	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256us pulse to host to report charger device status and fault.
OTG	8	I Digital	USB current limit selection pin during buck mode, and active high enable pin during boost mode. In buck mode with USB host, when OTG = High, IIN limit = 500mA and when OTG = Low, IIN limit = 100mA. The boost mode is activated when the REG01[5:4]=10 and OTG pin is High.
$\overline{CE}$	9	I Digital	Active low Charge Enable pin. Battery charging is enabled when REG01[5:4]=01 and $\overline{CE}$ pin = Low. $\overline{CE}$ pin must be pulled high or low.
ILIM	10	I Analog	ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1V. A resistor is connected from ILIM pin to ground to set the maximum limit as I_{INMAX} = (1V/R_{ILIM}) × 530. The actual input current limit is the lower one set by ILIM and by I^2C REG00[2:0]. The minimum input current programmed on ILIM pin is 500mA.
TS1	11	I Analog	Temperature qualification voltage input #1. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be shorted together.
TS2	12	I Analog	Temperature qualification voltage input #2. TS1 and TS2 pins have to be shorted together.
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. (Refer to Application Information Section for inductor and capacitor selection)

PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	O Analog	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047μF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047μF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. For VBUS above 6V, connect 1-μF ceramic capacitor from REGN to analog GND. For VBUS below 6V, connect a 4.7-μF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS1 and TS2 pins.
PMID	23	P	Battery Boost Mode Output Voltage. Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. The minimum capactiance required on PMID to PGND is 20uF (bq24195L) or 60uF (bq24195)
PowerPAD	–	P	Exposed pad beneath the IC for heat dissipation. Always solder PowerPAD™ to the board, and have vias on the Power Pad plane star-connecting to PGND and ground plane for high-current power converter.

ABSOLUTE MAXIMUM RATINGS

		VALUE
Voltage range (with respect to GND)	VBUS	–2 V – 20 V
	PMID, STAT,	–0.3 V –20 V
	BTST	–0.3 V – 26 V
	SW	–2 V – 20 V
	BAT, SYS (converter not switching)	–0.3 V – 6 V
	SDA, SCL, INT, OTG, ILIM, REGN, TS1, TS2, $\overline{CE}$, D+, D–	–0.3 V – 7 V
	BTST TO SW	–0.3 V – 7 V
	PGND to GND	–0.3 V – 0.3 V
Output sink current	INT, STAT	6mA
Junction temperature		–40°C to 150°C
Storage temperature		–65°C to 150°C

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.9	17(1)	V
I_{IN}	Input current		3	A
I_{SYS}	Output current (SYS)		4.5 (bq24195) 2.5 (bq24195L)	A
V_{BAT}	Battery voltage		4.4	V
I_{BAT}	Fast charging current		4.5 (bq24195) 2.5 (bq24195L)	A
	Discharging current with internal MOSFET		6 continuous 9 peak (up to 1 sec duration)	A
T_A	Operating free-air temperature range	–40	85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

THERMAL INFORMATION

THERMAL METRIC(1)		RGE PACKAGE 24-PIN	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	29.8	
θ_{JB}	Junction-to-board thermal resistance	9.1	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS)	$V_{VBUS} < V_{UVLO}$, VBAT = 4.2 V, leakage between BAT and VBUS			5	µA
		High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1)		12	20	µA
		High-Z Mode, or no VBUS, REG07[5] = 0, –40°C – 85°C		32	55	µA
I_{VBUS}	Input supply current (VBUS)	V_{VBUS} = 5 V, High-Z mode		15	30	µA
		V_{VBUS} = 17 V, High-Z mode		30	50	µA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT}=3.2V, I_{SYS}=0A		4		mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT}=3.8V, I_{SYS}=0A		15		mA
I_{BOOST}	Battery Discharge Current in boost mode	VBAT=4.2V, Boost mode, I_{PMID} = 0A, converter switching		15		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		17	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery	V_{VBUS} rising	3.6			V
V_{SLEEP}	Sleep mode falling threshold	V_{VBUS} falling, $V_{VBUS-VBAT}$	35	80	120	mV
V_{SLEEPZ}	Sleep mode rising threshold	V_{VBUS} rising, $V_{VBUS-VBAT}$	170	250	300	mV
V_{ACOV}	VBUS over-voltage rising threshold	V_{VBUS} rising	17.4	18		V
V_{ACOV_HYST}	VBUS Over-Voltage Falling Hysteresis	V_{VBUS} falling		700		mV
V_{BAT_UVLOZ}	Battery for active I^2C, no VBUS	V_{BAT} rising	2.3			V
V_{BAT_DPL}	Battery depletion threshold	V_{BAT} falling		2.4	2.6	V
$V_{BAT_DPL_HY}$	Battery depletion rising hysteresis	V_{BAT} rising		170	230	mV
$V_{VBUSMIN}$	Bad adapter detection threshold	V_{VBUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
t_{BADSRC}	Bad source detection duration			30		ms

ELECTRICAL CHARACTERISTICS (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER PATH MANAGEMENT						
V_{SYS_RANGE}	System regulation voltage	Isys = 0A, Q4 off, V_{BAT} up to 4.2 V, REG01[3:1]=101, V_{SYSMIN} = 3.5 V	3.5		4.35	V
V_{SYS_MIN}	System voltage output	REG01[3:1]=101, V_{SYSMIN} = 3.5 V	3.55	3.65		V
$R_{ON(RBFET)}$	Internal top reverse blocking MOSFET on-resistance	Measured between VBUS and PMID		23	38	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance between PMID and SW	T_J = –40°C – 85°C		30	38	mΩ
		T_J = -40°C – 125°C		30	48	
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between SW and PGND	T_J = –40°C – 85°C		35	48	mΩ
		T_J = -40°C – 125°C		35	51	
V_{FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10mA		30		mV
V_{SYS_BAT}	SYS/BAT Comparator	V_{SYS} falling		90		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising	3.4	3.55	3.7	V
V_{BATGD_HYST}	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
$V_{BAT_REG_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.208V	–0.5%		0.5%	
$I_{ICHG_REG_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.8V, I_{CHG} = 1792mA, T_J = 25°C	–4%		4%	
		V_{BAT} = 3.8V, I_{CHG} = 1792mA, T_J = –20°C – 125°C	–7%		7%	
I_{CHG_20pct}	Charge current with 20% option on	V_{BAT} = 3.1V, I_{CHG} = 104mA, REG02=03	75	100	125	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV_HYST}$	Battery LOWV rising threshold	Precharge to fast charge, REG04[1] = 1	2.8	3.0	3.1	V
I_{PRECHG_ACC}	Precharge current regulation accuracy	VBAT = 2.6V, I_{CHG} = 256mA	–20%		20%	
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 256mA, I_{CHG} = 960mA	–20%		20%	
V_{SHORT}	Battery Short Voltage	VBAT falling		1.8		V
V_{SHORT_HYST}	Battery Short Voltage hysteresis	VBAT rising		200		mV
I_{SHORT}	Battery short current	VBAT<2.2V		100		mA
V_{RECHG}	Recharge threshold below VBAT_REG	VBAT falling, REG04[0] = 0		100		mV
t_{RECHG}	Recharge deglitch time	VBAT falling, REG04[0]=0		20		ms
R_{ON_BATFET}	SYS-BAT MOSFET on-resistance	T_J = 25°C		12	15	mΩ
		T_J = –40°C – 125°C		12	20	
INPUT VOLTAGE/CURRENT REGULATION						
$V_{INDPM_REG_ACC}$	Input voltage regulation accuracy		–2%		2%	
I_{USB_DPM}	USB Input current regulation limit, VBUS = 5V, current pulled from SW	USB100	85		100	mA
		USB150	125		150	mA
		USB500	440		500	mA
		USB900	750		900	mA
I_{ADPT_DPM}	Input current regulation accuracy	Input current limit 1.5A	1.4	1.5	1.6	A
I_{IN_START}	Input current limit during system start up	VSYS<2.2V		100		mA
K_{ILIM}	$I_{IN} = K_{ILIM}/R_{ILIM}$	IINDPM = 1.5A	440	485	530	A x Ω
D+/D- DETECTION						
V_{D+_SRC}	D+ voltage source		0.5	0.6	0.7	V
I_{D+_SRC}	D+ connection check current source		7		14	µA
$I_{D–_SINK}$	D– current sink		50	100	150	µA
I_{D_LKG}	Leakage current into D+/D–	D–, switch open	–1		1	µA
		D+, switch open	–1		1	µA
V_{D+_LOW}	D+ Low comparator threshold		0.7		0.8	V
$V_{D–_LOWdatref}$	D– Low comparator threshold		250		400	mV
$R_{D–_DWN}$	D– Pulldown for connection check		14.25		24.8	kΩ
$t_{SDP_DEFAULT}$	Charging timer with 100mA USB host in default mode				45	mins

ELECTRICAL CHARACTERISTICS (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BAT OVER-VOLTAGE PROTECTION						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%		
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{Junction_REG}$	Junction temperature regulation accuracy	REG06[1:0] = 11	115	120	125	°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		160		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			30		°C
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
COLD/HOT THERMISTER COMPARATOR						
V_{LTF}	Cold temperature threshold, TS pin voltage rising threshold	Charger suspends charge. As Percentage to V_{REGN}	73%	73.5%	74%	
V_{LTF_HYS}	Cold temperature hysteresis, TS pin voltage falling	As Percentage to V_{REGN}	0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature TS pin voltage falling threshold	As Percentage to V_{REGN}	46.6%	47.2%	48.8%	
V_{TCO}	Cut-off temperature TS pin voltage falling threshold	As Percentage to V_{REGN}	44.2%	44.7%	45.2%	
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		10		ms
CHARGE OVER-CURRENT COMPARATOR						
I_{HSFET_OCP}	HSFET over-Current threshold		5.3	7		A
I_{BATFET_OCP}	System over load threshold		9			A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{LSFET_UCP}	LSFET charge under-current falling threshold	From sync mode to non-sync mode		100		mA
PWM OPERATION						
F_{SW}	PWM Switching frequency, and digital clock		1300	1500	1700	kHz
D_{MAX}	Maximum PWM duty cycle			97%		
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold	VBTST-VSW when LSFET refresh pulse is requested, VBUS=5V		3.6		V
		VBTST-VSW when LSFET refresh pulse is requested, VBUS>6V		4.2		V



ELECTRICAL CHARACTERISTICS (continued)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BOOST MODE OPERATION						
V_{OTG_REG}	Boost mode output voltage	I(PMID) = 0		5.12		V
$V_{OTG_REG_ACC}$	Boost mode output voltage accuracy	I(PMID) = 0	–2%		2%	
I_{OTG}	Boost mode output current on PMID	bq24195L	1.0			A
		bq24195	2.1			
V_{OTG_BAT}	Battery operating voltage for boost mode	bq24195L	3.0			V
		bq24195	3.2			V
V_{OTG_ILIM}	LSFET cycle-by-cycle current limit	bq24195L	2.76	3.8		A
		bq24195	4.83	6.5		
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 10V, I_{REGN} = 40mA	5.6	6	6.4	V
		V_{VBUS} = 5V, I_{REGN} = 20mA	4.75	4.8	4.85	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 10V, V_{REGN} = 3.8V	50			mA
LOGIC I/O PIN CHARACTERISTICS (OTG, $\overline{CE}$, STAT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
V_{OUT_LO}	Output low saturation voltage	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current	Pull up rail 1.8V			1	µA
I^2C INTERFACE (SDA, SCL, INT)						
V_{IH}	Input high threshold level	VPULL-UP = 1.8V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	VPULL-UP = 1.8V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{BIAS}	High-level leakage current	VPULL-UP = 1.8V, SDA and SCL			1	µA
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{HIZ}	Digital crude clock	REGN LDO disabled	15	35	50	kHz
f_{DIG}	Digital clock	REGN LDO enabled	1300	1500	1700	kHz
t_{WDT}	REG05[5:4]=11	REGN LDO enabled	136	160		sec

TYPICAL CHARACTERISTICS

Table 1. Tables of Figures

CHARGING EFFICIENCY
vs
CHARGING CURRENT

Efficiency (%)
Load Current (A)
VBUS = 5 V
VBUS = 7 V
VBUS = 9 V
VBUS = 12 V

Figure 1.

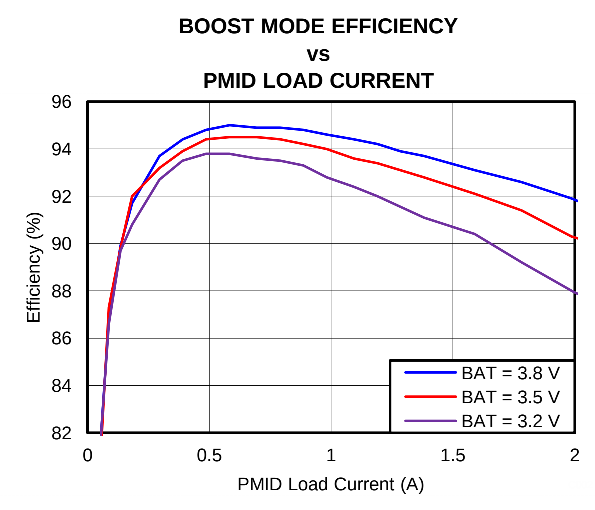


Figure 2.

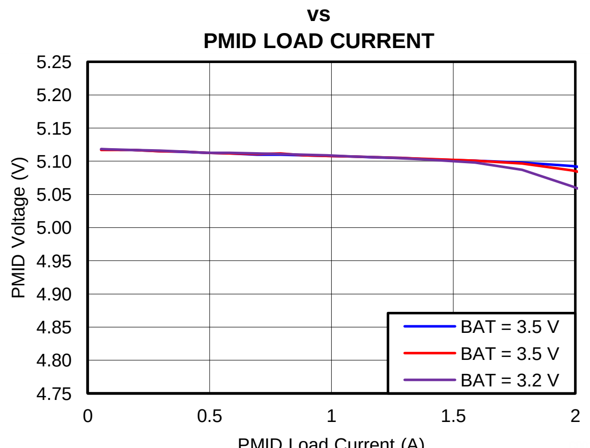
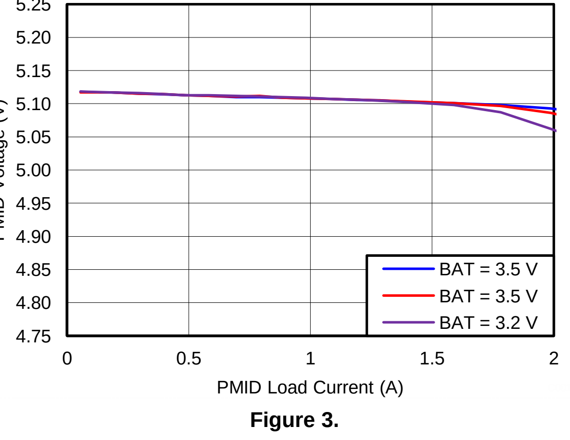



Figure 3.

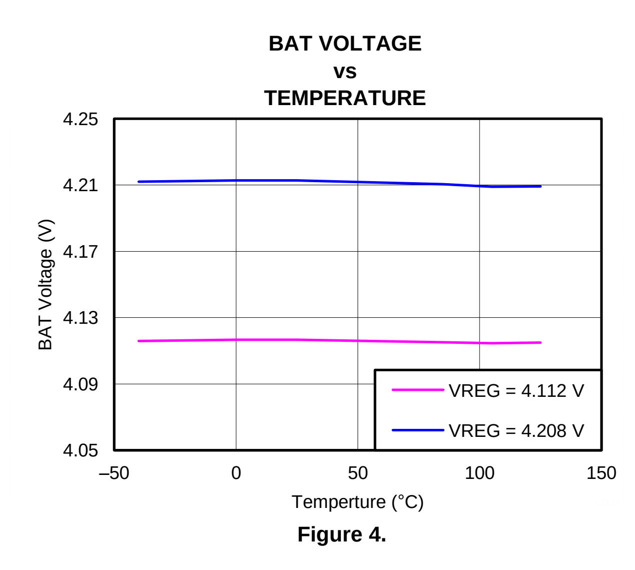


Figure 4.

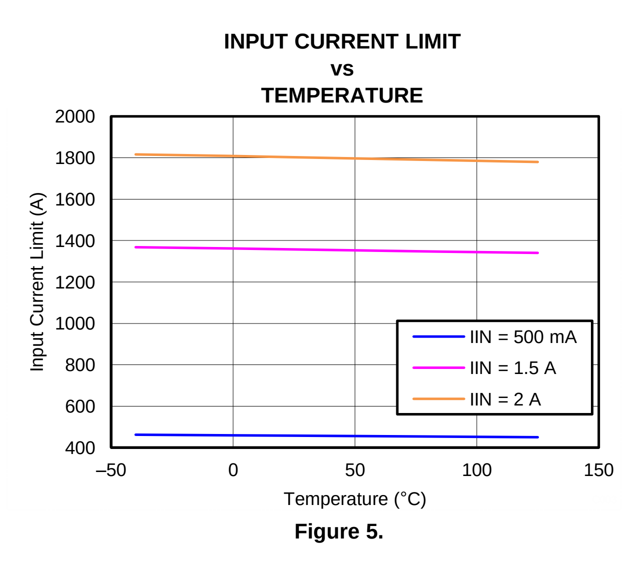


Figure 5.

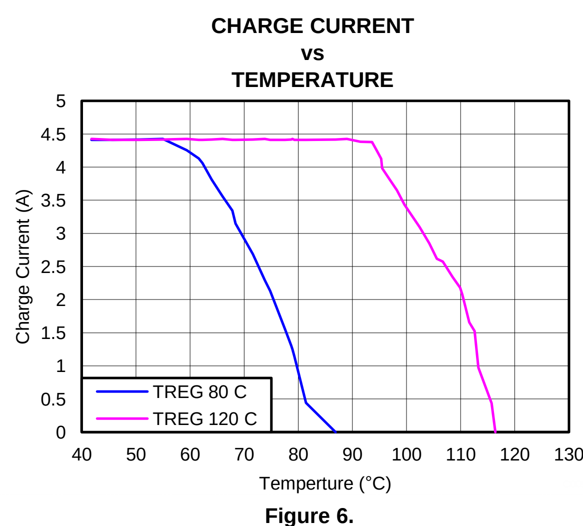


Figure 6.

Power Up from USB100mA (VBAT 3.2V)

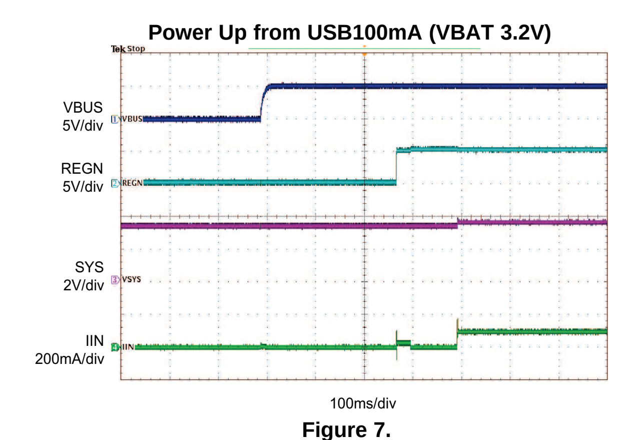


Figure 7.

Charge Enable (VBUS 5V)

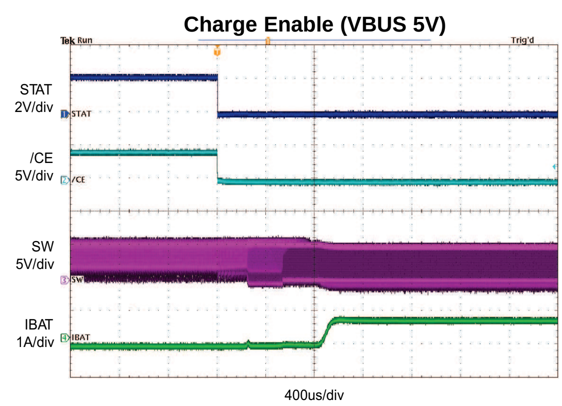
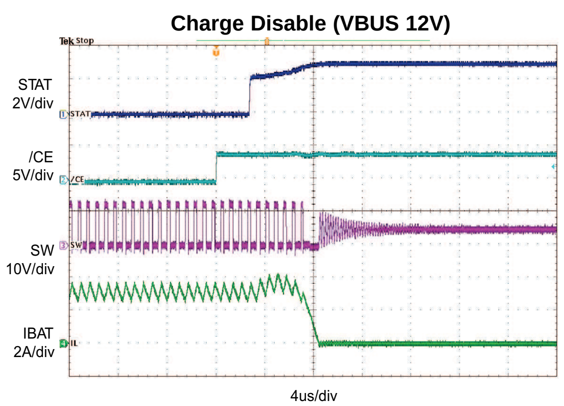


Figure 8.

Charge Disable (VBUS 12V)



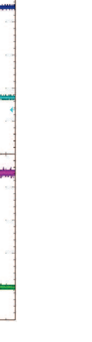


Figure 9.

Input Current DPM Response without Battery (VBUS 5V, IIN 3A, Charge Disable)

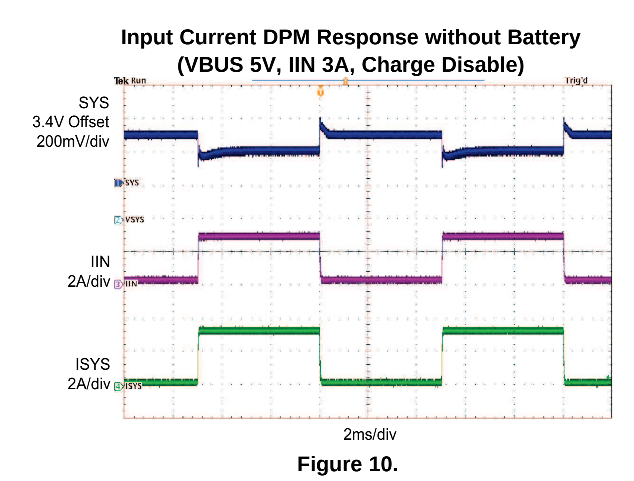


Figure 10.

PWM Switching Waveform (VBUS 12V, VBAT 3.8V, ICHG 3A)

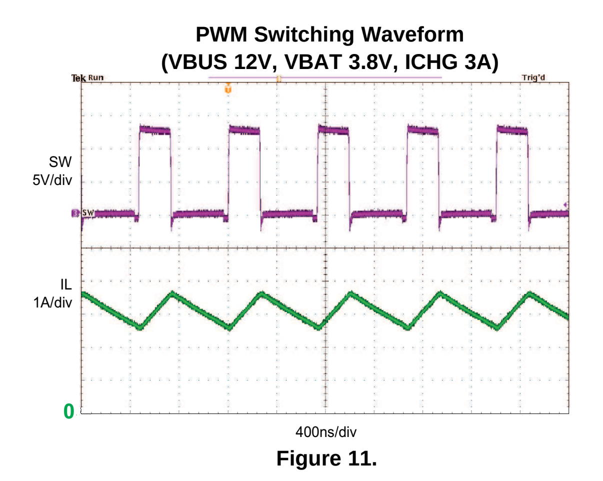


Figure 11.

PFM Switching Waveform (VBUS 9V, No Battery, ISYS 10 mA, Charge Disable)

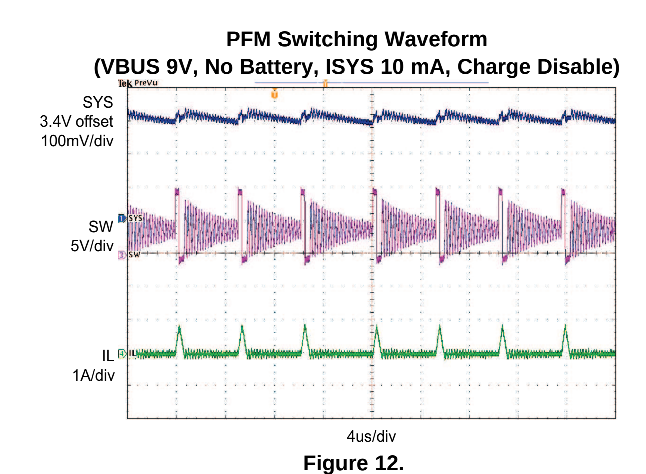


Figure 12.

Boost Mode Switching Waveform (VBAT 3.8V, ILOAD 1A)

SW
5V/div

IL
1A/div

400ns/div

Figure 13.

Boost Mode Load Transient (VBAT 3.8V)

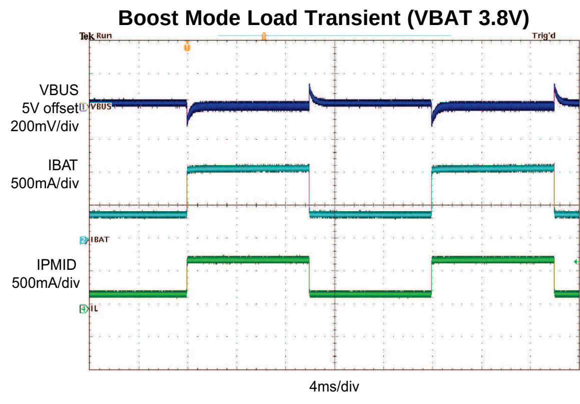


Figure 14.



I²C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are read only.

Input Source Control Register REG00 (default 00110000, or 30)

BIT		DESCRIPTION	
Bit 7	EN_HIZ	0 – Disable, 1 – Enable	Default: Disable (0)
Input Voltage Limit			
Bit 6	VINDPM[3]	640mV	Offset 3.88V, Range: 3.88V-5.08V Default: 4.36V (0110)
Bit 5	VINDPM[2]	320mV	
Bit 4	VINDPM[1]	160mV	
Bit 3	VINDPM[0]	80mV	
Input Current Limit (Actual input current limit is the lower of I²C and ILIM)			
Bit 2	IINLIM[2]	000 – 100mA, 001 – 150mA, 010 – 500mA, 011 – 900mA, 100 – 1.2A, 101 – 1.5A, 110 – 2A, 111 – 3A	Default SDP: 100mA (000)(OTG pin=0) or 500mA (010) (OTG pin=1) Default DCP/CDP: 1.5A (101)
Bit 1	IINLIM[1]		
Bit 0	IINLIM[0]		

Power-On Configuration Register REG01 (default 00011011, or 1B)

BIT		DESCRIPTION	NOTE
Bit 7	Register Reset	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Back to 0 after register reset
Bit 6	I²C Watchdog Timer Reset	0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after timer reset
Charger Configuration			
Bit 5	CHG_CONFIG[1]	00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG	Default: Charge Battery (01)
Bit 4	CHG_CONFIG[0]		
Minimum System Voltage Limit			
Bit 3	SYS_MIN[2]	0.4V	Offset: 3.0V, Range 3.0V-3.7V Default: 3.5V (101)
Bit 2	SYS_MIN[1]	0.2V	
Bit 1	SYS_MIN[0]	0.1V	
Bit 0	Reserved	1 - Reserved	

Charge Current Control Register REG02 (default 01100000, or 60)

BIT		DESCRIPTION	NOTE
Fast Charge Current Limit			
Bit 7	ICHG[5]	2048mA	Offset: 512mA Range: 512-4544mA (bq24195) Range: 512-2496mA (bq24195L) Default: 2048mA (011000)
Bit 6	ICHG[4]	1024mA	
Bit 5	ICHG[3]	512mA	
Bit 4	ICHG[2]	256mA	
Bit 3	ICHG[1]	128mA	
Bit 2	ICHG[0]	64mA	
Bit 1	Reserved	0 - Reserved	
Bit 0	FORCE_20PCT	0 – ICHG as REG02[7:2] programmed 1 – ICHG as 20% of REG02[7:2] programmed	Default: ICHG as REG02[7:2] programmed (0)

Pre-Charge/Termination Current Control Register REG 03 (default 00010001, or 11)

BIT		DESCRIPTION	NOTE
Pre-Charge Current Limit			
Bit 7	IPRECHG[3]	1024mA	Offset: 128mA, Range: 128mA – 2048mA Default: 256mA (0001)
Bit 6	IPRECHG[2]	512mA	
Bit 5	IPRECHG[1]	256mA	
Bit 4	IPRECHG[0]	128mA	
Termination Current Limit			
Bit 3	ITERM[3]	1024mA	Offset: 128mA Range: 128mA – 2048mA Default: 256mA (0001)
Bit 2	ITERM[2]	512mA	
Bit 1	ITERM[1]	256mA	
Bit 0	ITERM[0]	128mA	

Charge Voltage Control Register REG04 (default 10110010, or B2)

BIT		DESCRIPTION	NOTE
Charge Voltage Limit			
Bit 7	VREG[5]	512mV	Offset: 3.504V Range: 3.504V – 4.400V (111000) Default: 4.208V (101100)
Bit 6	VREG[4]	256mV	
Bit 5	VREG[3]	128mV	
Bit 4	VREG[2]	64mV	
Bit 3	VREG[1]	32mV	
Bit 2	VREG[0]	16mV	
Battery Precharge to Fast Charge Threshold			
Bit 1	BATLOWV	0 – 2.8V, 1 – 3.0V	Default: 3.0V (1)
Battery Recharge Threshold (below battery regulation voltage)			
Bit 0	VRECHG	0 – 100mV, 1 – 300mV	Default: 100mV (0)

Charge Termination/Timer Control Register REG05 (default 10011010, or 9A)

BIT		DESCRIPTION	NOTE
Charging Termination Enable			
Bit 7	EN_TERM	0 – Disable, 1 – Enable	Default: Enable termination (1)
Termination Indicator Threshold			
Bit 6	TERM_STAT	0 – Match ITERM, 1 – STAT pin high before actual termination when charge current below 800 mA	Default Match ITERM (0)
I2C Watchdog Timer Setting			
Bit 5	WATCHDOG[1]	00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s	Default: 40s (01)
Bit 4	WATCHDOG[0]		
Charging Safety Timer Enable			
Bit 3	EN_TIMER	0 – Disable, 1 – Enable	Default: Enable (1)
Fast Charge Timer Setting			
Bit 2	CHG_TIMER[1]	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 8hours (01) (See Charging Safety Timer for details)
Bit 1	CHG_TIMER[0]		
Bit 0	Reserved	0 - Reserved	





Thermal Regulation Control Register REG06 (default 00000011, or 03)

BIT		DESCRIPTION	NOTE
Bit 7	Reserved	0 - Reserved	
Bit 6	Reserved	0 - Reserved	
Bit 5	Reserved	0 - Reserved	
Bit 4	Reserved	0 - Reserved	
Bit 3	Reserved	0 - Reserved	
Bit 2	Reserved	0 - Reserved	
Thermal Regulation Threshold			
Bit 1	TREG[1]	00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C	Default: 120°C (11)
Bit 0	TREG[0]		

Misc Operation Control Register REG07 (default 01001011, or 4B)

BIT		DESCRIPTION	NOTE
Force DPDM detection			
Bit 7	DPDM_EN	0 – Not in D+/D– detection; 1 – Force D+/D– detection	Default: Not in D+/D– detection (0), Back to 0 after detection complete
Safety Timer Setting during Input DPM and Thermal Regulation			
Bit 6	TMR2X_EN	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
Force BATFET Off			
Bit 5	BATFET_Disable	0 – Allow Q4 turn on, 1 – Turn off Q4	Default: Allow Q4 turn on(0)
Bit 4	Reserved	0 - Reserved	
Bit 3	Reserved	1 - Reserved	
Bit 2	Reserved	0 - Reserved	
Bit 1	INT_MASK[1]	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

System Status Register REG08

BIT		DESCRIPTION
Bit 7	VBUS_STAT[1]	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	
Bit 5	CHRG_STAT[1]	00 – Not Charging, 01 – Pre-charge (<$V_{BATLOWV}$), 10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	
Bit 3	DPM_STAT	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	0 – Normal, 1 – In Thermal Regulation
Bit 0	VSYS_STAT	0 – Not in VSYSMIN regulation (BAT>VSYSMIN), 1 – In VSYSMIN regulation (BAT<VSYSMIN)

Fault Register REG09

BIT		DESCRIPTION
Bit 7	WATCHDOG_FAULT	0 – Normal, 1- Watchdog timer expiration
Bit 6	Reserved	0 - Reserved
Bit 5	CHRG_FAULT[1]	00 – Normal, 01 – Input fault (VBUS OVP or VBAT<VBUS<3.8V), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration
Bit 4	CHRG_FAULT[0]	
Bit 3	BAT_FAULT	0 – Normal, 1 – BATOVP
Bit 2	NTC_FAULT[2]	000 – Normal, 101 – Cold, 110 – Hot
Bit 1	NTC_FAULT[1]	
Bit 0	NTC_FAULT[0]	

Vender / Part / Revision Status Register REG0A

BIT		DESCRIPTION
Bit 7	Reserved	0 - Reserved
Bit 6	Reserved	0 - Reserved
Device Configuration		
Bit 5	PN[2]	100
Bit 4	PN[1]	
Bit 3	PN[0]	
Bit 2	TS_PROFILE	0 - Cold/Hot window
Bit 1	DEV_REG[0]	11
Bit 0	DEV_REG[1]	

DETAILED DESCRIPTION

The bq24195L, bq24195 is an I^2C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

Device Power Up

Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DEPL}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

BATFET Turn Off

The BATFET can be forced off by the host through I^2C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery.

When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

Shipping Mode

When end equipment is assembled, the system is connected to battery through BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage.

In order to keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4]=00) and disable BATFET (REG07[5]=1) at the same time.

Once the BATFET is disabled, the BATFET can be turned on by plugging in adapter.

Power Up from DC Source

When the DC source plugs in, the bq24195L, bq24195 checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS1/TS2 external resistors. The pull-up rail of STAT can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.

1. VBUS above UVLOZ
2. VBUS above battery + V_{SLEEPZ} in buck mode or VBUS below battery + V_{SLEEPZ} in boost mode
3. After typical 220ms delay (100ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than 50µA from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

Input Source Qualification

After REGN LDO powers up, the bq24195L, bq24195 checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below 18V (not in ACOV)
2. VBUS voltage above 3.8V when pulling 30mA (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 1.5A.

After REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The bq24195L, bq24195 follows battery charging specification 1.2 (bc1.2) to detect input source through USB D+/D– lines. After the input current limit detection is done, the host can write to REG00[2:0] to change the input current limit.

D+/D– Detection Sets Input Current Limit

The bq24195L, bq24195 contains a D+/D– based input source detection to program the input current limit. The D+/D- detection has two steps: data contact detect (DCD) followed by primary detection.



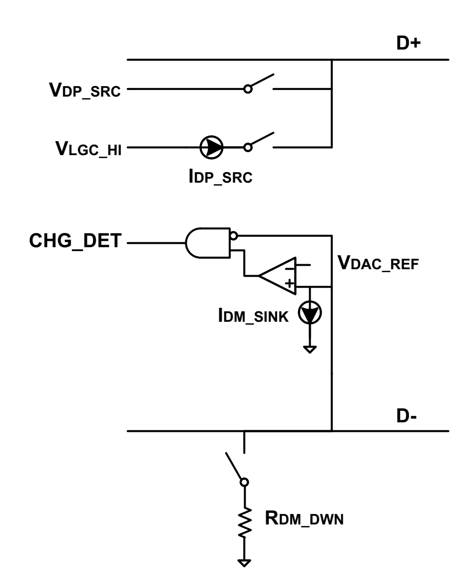


Figure 15. USB D+/D- Detection

DCD (Data Contact Detection) uses a current source to detect when the D+/D– pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and REG08[2]=1 (power good)
- Turn on D+ I_{DP_SRC} and the D– pull-down resistor R_{DM_DWN} for 40ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec.
- Turn off I_{DP_SRC} and disconnect R_{DM_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V_{DP_SRC} on D+ and I_{DM_SINK} on D– for 40ms
- If PD is attached to a USB host (SDP), the D– is low. If PD is attached to a charging port (CDP or DCP), the D– is high
- Turn off V_{DP_SRC} and I_{DM_SINK}

Table 2 shows the input current limit setting after D+/D– detection.

Table 2. bq24195L, bq24195 USB D+/D– Detection

D+/D– DETECTION	OTG	INPUT CURRENT LIMIT	REG08[7:6]
0.5 sec timer expired in DCD (D+/D- floating)	—	100 mA	00
USB Host	LOW	100 mA	01
USB Host	HIGH	500 mA	01
Charging Port	—	1.5 A	10

HIZ State wth 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100mA USB host, and the battery is above bat-good threshold (V_{BATGD}), the device follows battery charging spec and enters high impedance state (HIZ). In HIZ state, the device is in the lowest quiescent state with REGN LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be less than 30µA. The system is supplied by the battery.

Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7]=0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.



In default mode, the charger IC will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

Force Input Current Limit Detection

The host can force the charger device to run input current limit detection by setting REG07[7]=1. After the detection is complete, REG07[7] will return to 0 by itself.

Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The bq24195L, bq24195 provides soft-start when ramp up the system rail. When the system rail is below 2.2V, the input current limit is forced to 100mA. After the system rises above 2.2V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

As a battery charger, the bq24195L, bq24195 deploys a 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

Boost Mode Operation from Battery

The bq24195L, bq24195 supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the 1A (bq24195L) or 2.1A (bq24195) charging requirements for smartphone and tablet. The boost operation can be enabled if the following conditions are valid:

1. BAT above BATLOWV threshold ($V_{BATLOWV}$ set by REG04[1])
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)
3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4]=10)
4. After 220ms delay from boost mode enable

In battery boost mode, the bq24195L, bq24195 employs a 1.5MHz step-up switching regulator. During boost mode, the status register REG08[7:6] is set to 11, the PMID output voltage is 5.1V.

For power bank applications, the boost current is supported from PMID pin as in the application diagram. It is recommended to use the minimum PMID cap value 20uF (bq24195L) or 60uF (bq24195) for boost current. Please note that there is no boost current limit setting when the boost current is sourced from PMID pin, hence it is important not to overload the boost current under this condition.

Power Path Management

The bq24195L, bq24195 accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

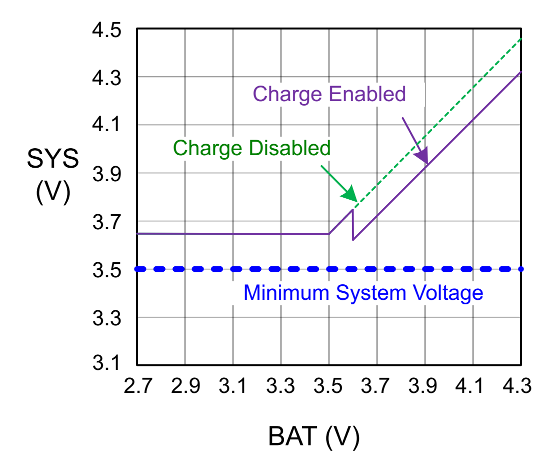


Figure 16. V(SYS) vs V(BAT)

Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the bq24195L, bq24195 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

Figure 17 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current and 3.4V minimum system voltage setting.



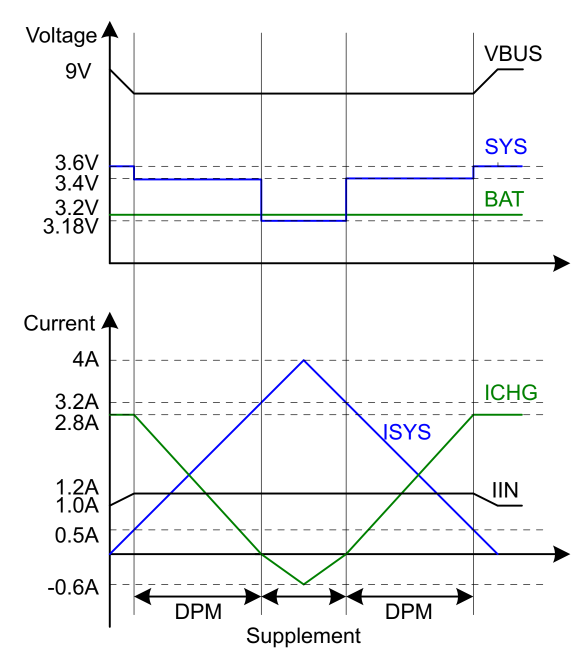


Figure 17. DPM Response

Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. Figure 18 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

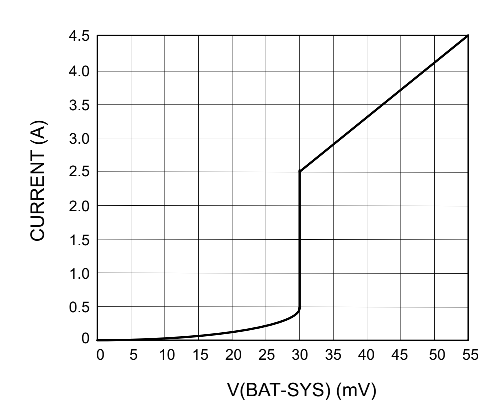


Figure 18. BATFET V-I Curve

Battery Charging Management

The bq24195L, bq24195 charges 1-cell Li-Ion battery with up to 2.5A/4.5A charge current for high capacity tablet battery. The 12mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the bq24195L, bq24195 can complete a charging cycle without host involvement. The device default charging parameters are listed in .

Table 3. Charging Parameter Default Setting

DEFAULT MODE	bq24195L, bq24195
Charging Voltage	4.208 V
Charging Current	2.036 A
Pre-charge Current	256 mA
Termination Current	256 mA
Temperature Profile	Hot/Cold
Safety Timer	8 hours(1)

(1) See section Charging Safety Timer for more information.

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by I²C register bit (REG01[5:4]) = 01 and $\overline{CE}$ is low
- No thermistor fault on TS1 and TS2
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the bq24195L, bq24195 automatically starts another charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I²C.

Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

Table 4. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
<2V	100mA	–	01
2V-3V	REG03[7:4]	256mA	01
>3V	REG02[7:2]	2048mA	10



If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

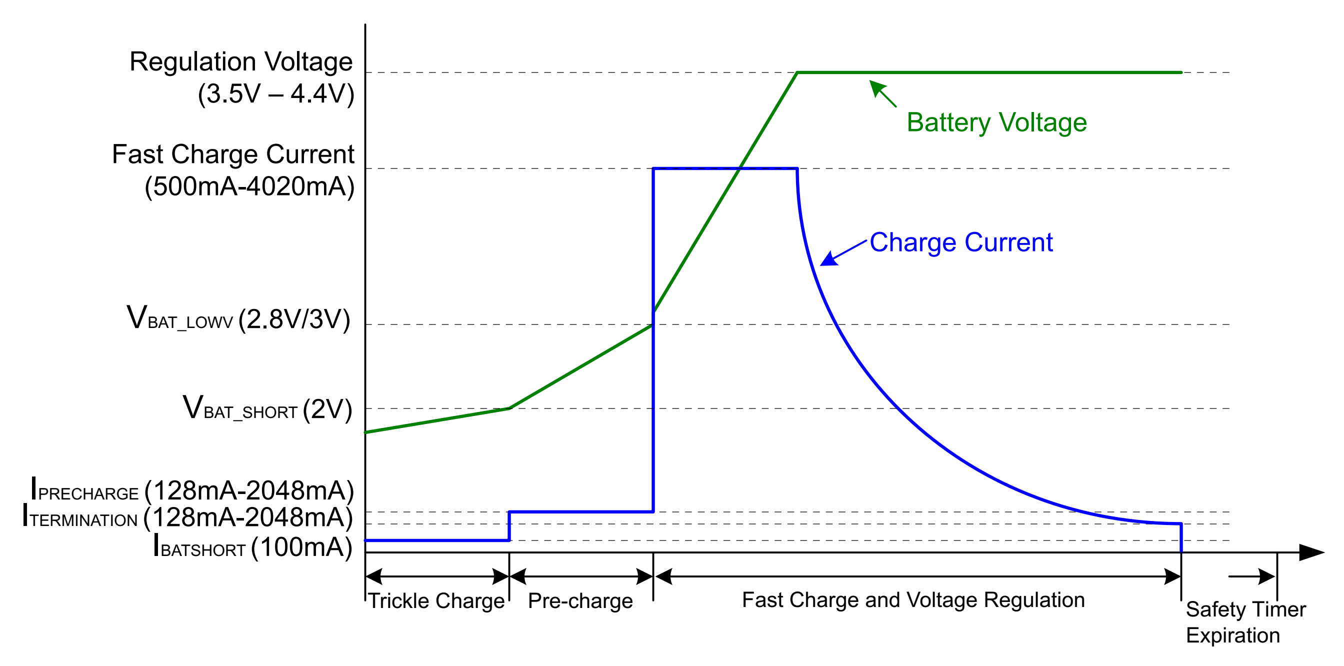


Figure 19. Battery Charging Profile

Thermistor Cold/Hot Temperature Window

The bq24195L, bq24195 continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

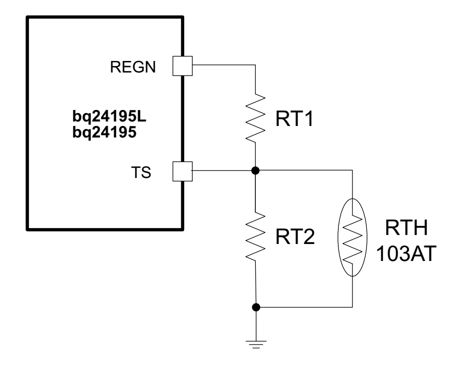


Figure 20. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

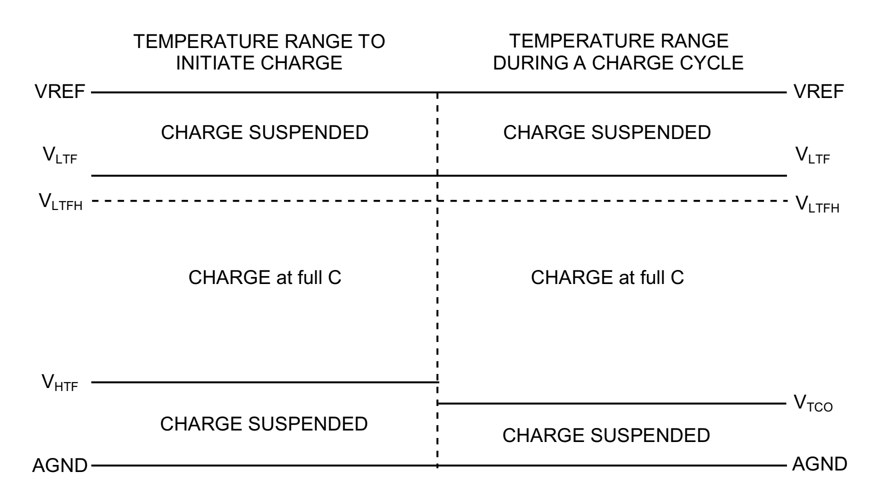


Figure 21. TS Pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor is used on the battery pack , the value RT1 and RT2 can be determined by using the following equation:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (1)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.52 kΩ
RT2 = 31.23 kΩ

Charging Termination

The bq24195L, bq24195 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG09[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

Termination when REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through $\overline{CE}$ pin or REG01[5:4].

Termination when REG05[6] = 1

Usually the STAT bit indicates charging complete when the charging current falls below termination threshold. Write REG05[6]=1 to enable an early "charge done" indication on STAT pin. The STAT pin goes high when the charge current reduces below 800mA. The charging cycle is still on-going until the current falls below the termination threshold.

Charging Safety Timer

The bq24195L, bq24195 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

In default mode, the device keeps charging the battery with 5-hour fast charging safety timer regardless of REG05[2:1] default value. At the end of the 5 hours, the EN_HIZ (REG00[7]) is set to signal the buck converter stops and the system load is supplied by the battery. The EN_HIZ bit can be cleared to restart the buck converter.

In host mode, the device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the REG05[2:1] bits (default = 8 hours). At the end of safety timer, the EN_HIZ (REG00[7]) is cleared to signal the buck converter continues to operation to supply system load.

The safety timer is 1 hour when the battery is below BATLOWV threshold. The user can program fast charge safety timer through I^2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C (REG05[3]).

The following actions restart the safety timer:

- At the beginning of a new charging cycle
- Toggle the $\overline{CE}$ pin HIGH to LOW to HIGH (charge enable)
- Write REG01[5:4] from 00 to 01 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)
- Write REG01[7] to 1 (software reset)

During input voltage/current regulation or thermal regulation, the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

Host Mode and Default Mode

The bq24195L, bq24195 is a host controlled device, but it can operate in default mode without host management. In default mode, bq24195L, bq24195 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings.

Any write command to bq24195L, bq24195 transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4]=11.



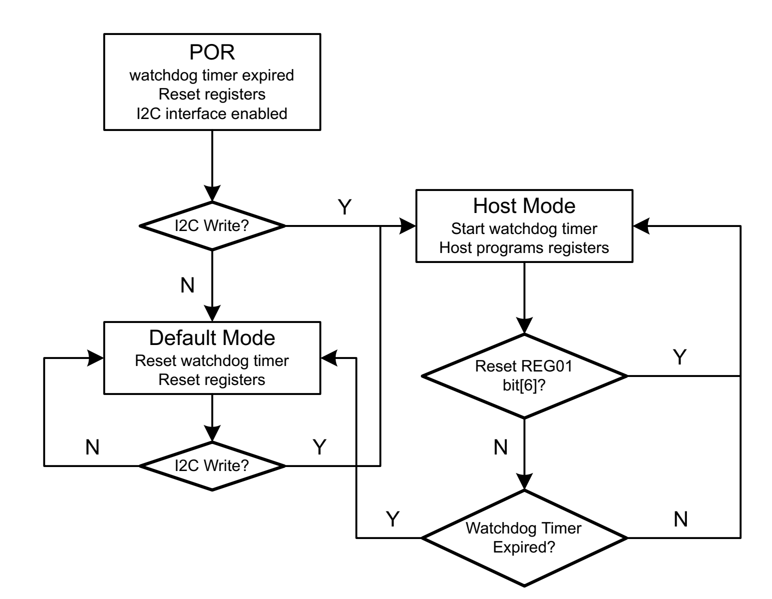


Figure 22. Watchdog Timer Flow Chart

Plug in USB100mA Source with Good Battery

When the input source is detected as 100mA USB host, and the battery voltage is above batgood threshold (V_{BATGD}), the charger device enters HIZ state to meet the battery charging spec requirement.

If the charger device is in host mode, it will stay in HIZ state even after the USB100mA source is removed, and the adapter plugs in. During the HIZ state, REG00[7] is set HIGH and the system load is supplied from battery. It is recommended that the processor host always checks if the charger IC is in HIZ state when it wakes up. The host can write REG00[7] to 0 to exit HIZ state.

If the charger is in default mode, when the DC source is removed, the charger device will get out of HIZ state automatically. When the input source plugs in again, the charger IC runs detection on the input source and update the input current limit.

USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

Status Outputs (STAT and INT)

Charging Status Indicator (STAT)

The bq24195L, bq24195 indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.



Table 5. STAT Pin State

CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault, input or system over-voltage)	blinking at 1Hz

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256us INT pulse.

- USB/adapter source identified (through DPDM detection)
- Good input source detected
  - not in sleep
  - not in ACOV
  - current limit above 30mA
- Input removed or ACOV
- Charge Complete
- Any FAULT event in REG09

When a fault occurs, the charger device sends out INT and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1^{st} reads fault register status from the last INT and the 2^{nd} reads the current fault register status.

Protections

Input Current Limit on ILIM

For safe operation, the bq24195L, bq24195 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times 530 \quad (2)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 353Ω resistor to ground for 1.5A, the input current limit is 1.5A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1V. If ILIM voltage exceeds 1V, the device enters input current regulation (Refer to *Dynamic Power Path Management* section).

The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following Equation 3:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (3)$$

For example, if ILIM pin sets 2A, and the ILIM voltage is 0.6V, the actual input current 1.2A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1V. If ILIM pin is short, the input current limit is set by the register.

Thermal Regulation and Thermal Shutdown

The bq24195L, bq24195 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.



During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

Voltage and Current Monitoring in Buck Mode

The bq24195L, bq24195 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is 18V. If VBUS voltage exceeds 18V, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

System Over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

Current Monitoring in Boost Mode

The bq24195L, bq24195 closely monitors LSFET current to ensure safe boost mode operation.

Battery Protection

Battery Over-Current Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[5] goes high and an INT is asserted to the host.

Charging During Battery Short Protection

If the battery voltage falls below 2V, the charge current is reduced to 100mA for battery safety.

System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the BATFET is latched off. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.

Serial Interface

The bq24195L, bq24195 uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I2C™ is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I^2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

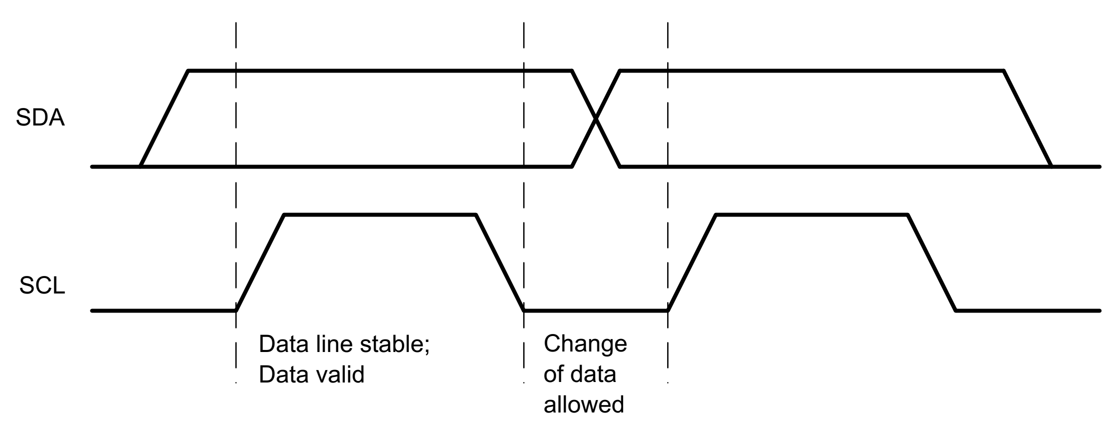


Figure 23. Bit Transfer on the I²C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

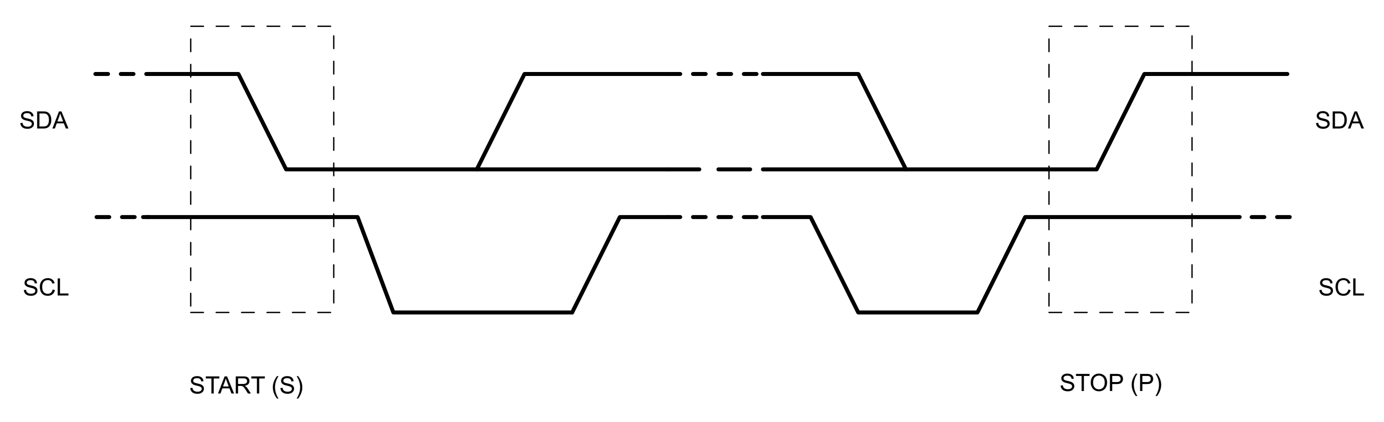


Figure 24. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

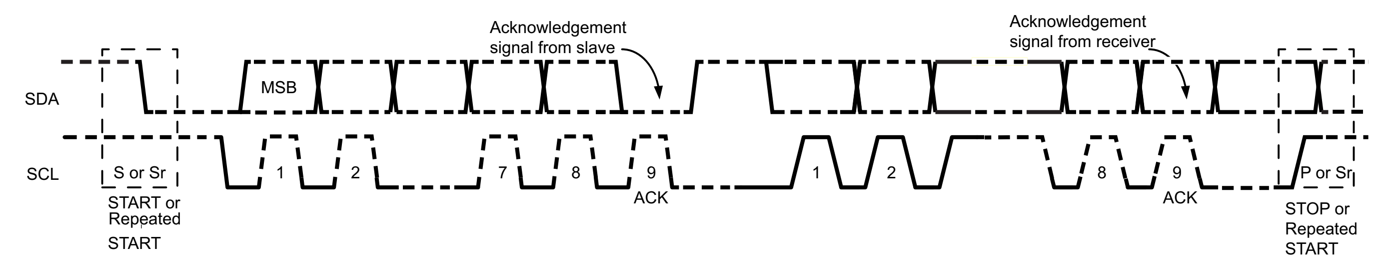


Figure 25. Data Transfer on the I²C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

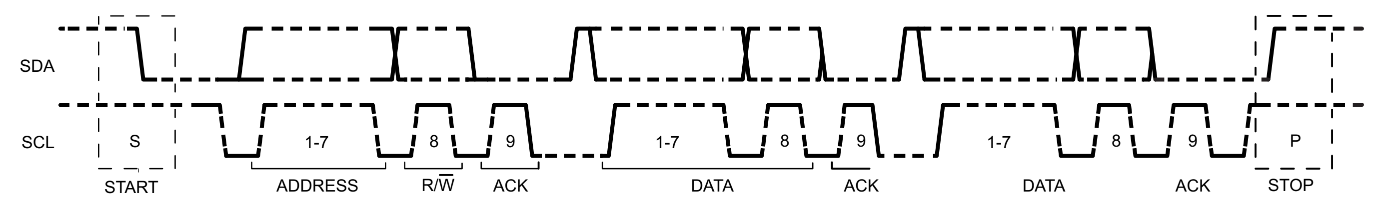


Figure 26. Complete Data Transfer

Single Read and Write

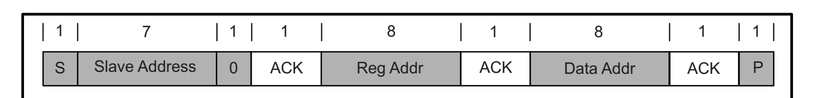


Figure 27. Single Write

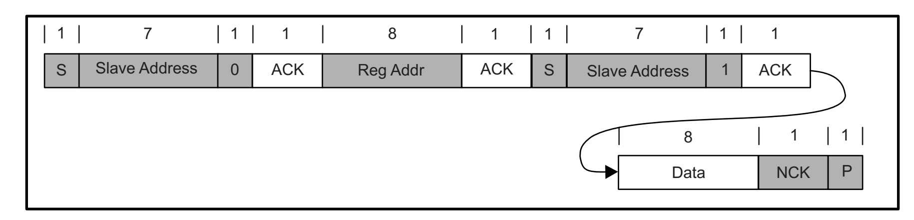


Figure 28. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

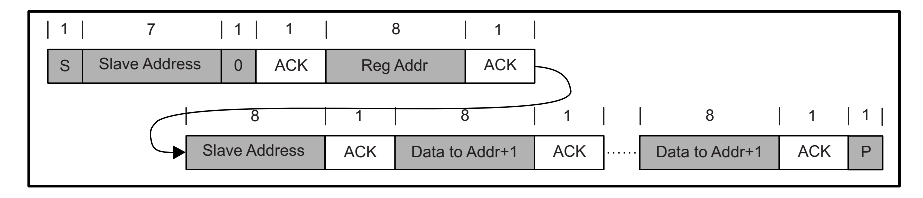


Figure 29. Multi-Write

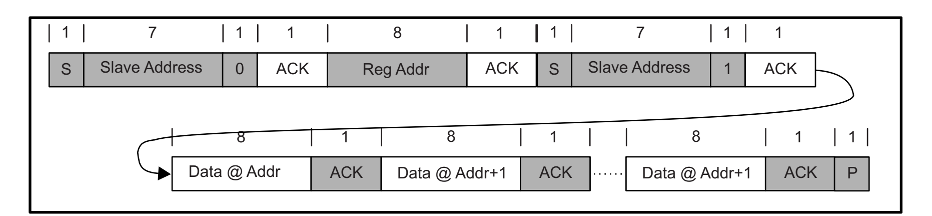


Figure 30. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.



APPLICATION INFORMATION

Inductor Selection

The bq24195L, bq24195 has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (VBUS), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Typical inductor value is 2.2µH.

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (6)$$

For best performance, VBUS should be decouple to PGND with 1µF capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 15V input voltage.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LC fs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15kHz and 25kHz. With 2.2µH inductor, the typical output capacitor value is 20µF. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 31) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, refer to SCBA017 and SLUA271.

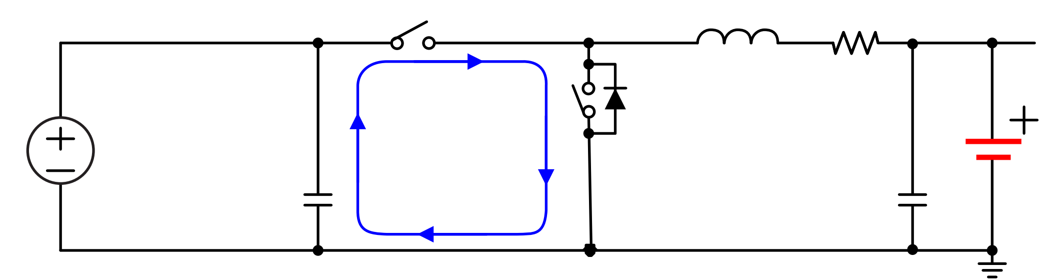


Figure 31. High Frequency Current Path

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ24195LRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24195LRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24195RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24195RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

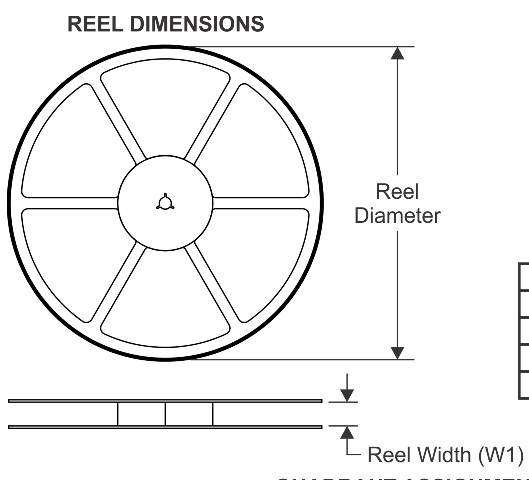
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

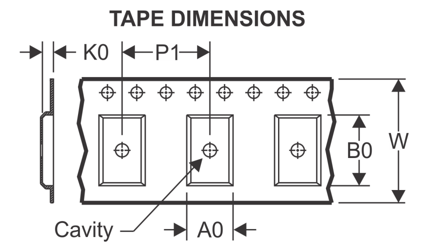
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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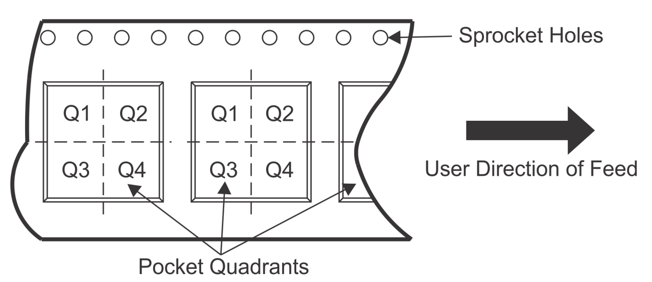
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

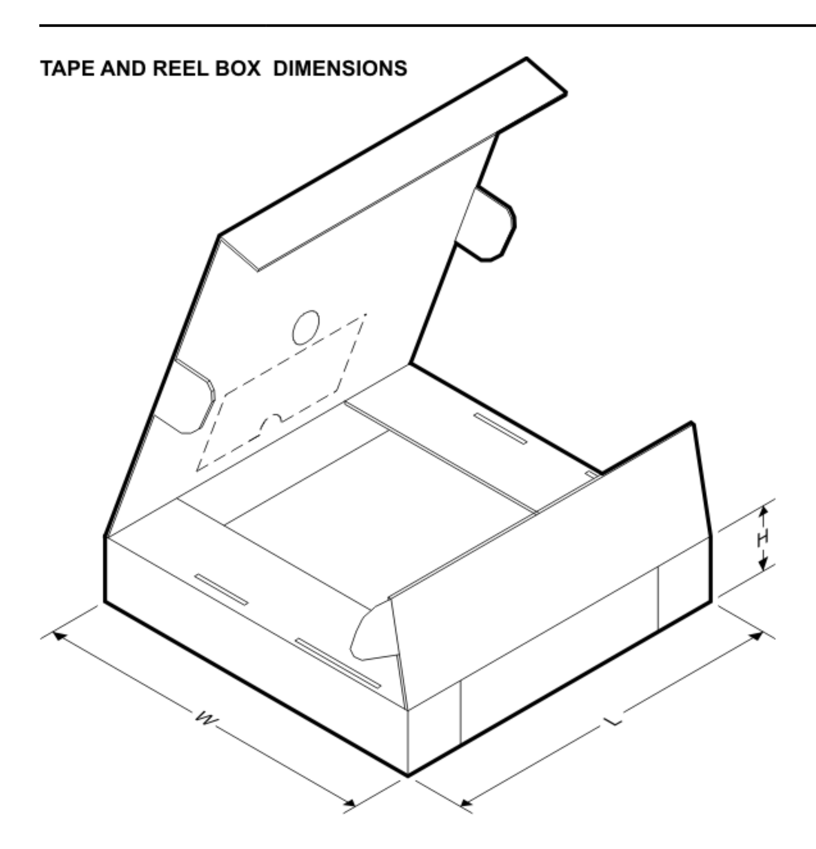
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24195LRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195LRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24195LRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24195LRGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24195RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24195RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

4,15
3,85
A
B
4,15
3,85
PIN 1 INDEX AREA
TOP AND BOTTOM

1,00
0,80
0,20 REF.
SEATING PLANE
0,08
C
0,05
0,00

0,50
24X 0,50
0,30
1
6
24
7
THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET
19
12
18
13
24X 0,30
0,18

⌖	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

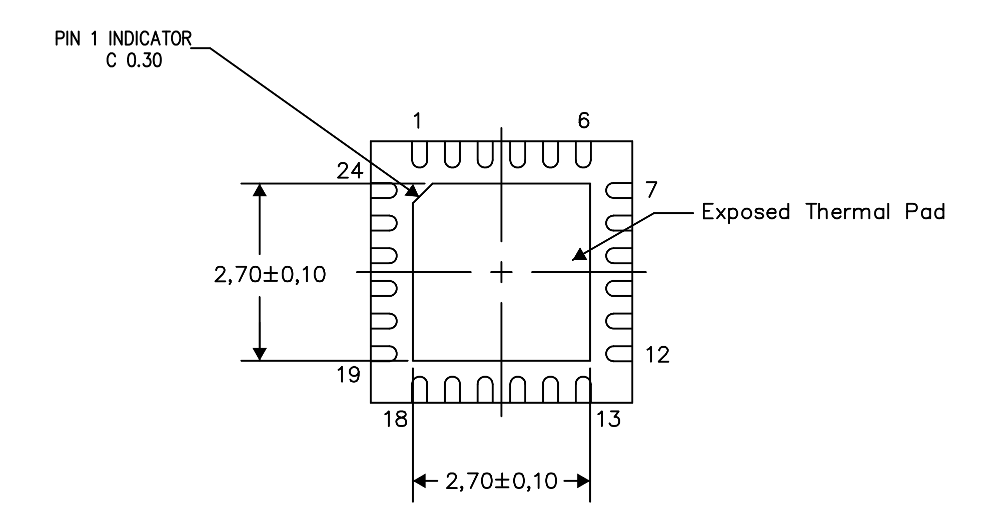
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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NOTES: A. All linear dimensions are in millimeters



RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

Note D
20x0,5
3,1 4,8
3,1
4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5
24x0,8
4x1,1
0,3
24x0,23
0,3
4x1,1
R0,115
3,15 4,75
3,15
4,75
(66% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08
R0,14
0,85
Pad Geometry
(Note C)
0,28
0,07
All Around

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,7
9xØ0,3
6x0,9
2,7
6x0,9

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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